FAIRCHILD SEMICONDUCTOR®

November 2003

FDC6020C

Complementary PowerTrench® MOSFET

General Description

These N & P-Channel MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

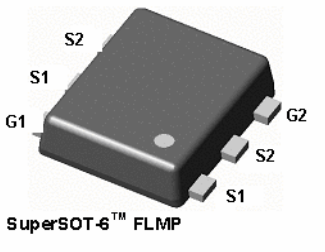
These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

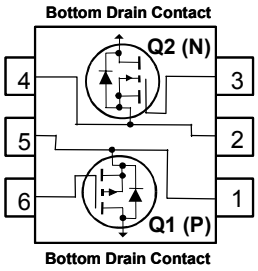
Applications

- DC/DC converter
- Load switch
- Motor Driving

Features

- **Q1** –4.2 A, –20V. $R_{DS(ON)}$ = 55 mΩ @ V_{GS} = – 4.5 V
  $R_{DS(ON)}$ = 82 mΩ @ V_{GS} = – 2.5 V
- **Q2** 5.9 A, 20V. $R_{DS(ON)}$ = 27 mΩ @ V_{GS} = 4.5 V
  $R_{DS(ON)}$ = 39 mΩ @ V_{GS} = 2.5 V
- Low gate charge
- High performance trench technology for extremely low $R_{DS(ON)}$.
- FLMP SSOT-6 package: Enhanced thermal performance in industry-standard package size





Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		Q1	Q2	Units
V_{DSS}	Drain-Source Voltage		–20	20	V
V_{GSS}	Gate-Source Voltage		±12	±12	V
I_D	Drain Current - Continuous	(Note 1a)	–4.2	5.9	A
	- Pulsed		–20	20	
P_D	Power Dissipation for Dual Operation	(Note 1a)	1.6		W
	Power Dissipation for single Operation	(Note 1a)	1.8		
		(Note 1b)	1.2		
T_J, T_{STG}	Operating and Storage Junction Temperature Range		–55 to +150		°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	68	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1a)	1	

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
.020	FDC6020C	7''	8mm	3000 units

Electrical Characteristics

T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Off Characteristics							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = –250 µA V_{GS} = 0 V, I_D = 250 µA	Q1 Q2	–20 20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = –250 µA, Referenced to 25°C I_D = 250 µA, Referenced to 25°C	Q1 Q2		–14 12		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = –16 V, V_{GS} = 0 V V_{DS} = 16 V, V_{GS} = 0 V	Q1 Q2			–1 1	µA
I_{GSS}	Gate-Body Leakage	V_{GS} = ±12 V, V_{DS} = 0 V V_{GS} = ±12 V, V_{DS} = 0 V	Q1 Q2			±100 ±100	nA
On Characteristics (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = –250 µA V_{DS} = V_{GS}, I_D = 250 µA	Q1 Q2	–0.6 0.6	–1.0 1.0	–1.5 1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = –250 µA, Referenced to 25°C I_D = 250 µA, Referenced to 25°C	Q1 Q2		3 –3		mV/°C
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = –4.5 V, I_D = –4.2 A V_{GS} = –2.5 V, I_D = –3.4 A V_{GS} = –4.5 V, I_D = –4.2 A, T_J =125°C	Q1		45 65 58	55 82 73	mΩ
		V_{GS} = 4.5 V, I_D = 5.9 A V_{GS} = 2.5 V, I_D = 4.9 A V_{GS} = 4.5 V, I_D = 5.9 A, T_J = 125°C	Q2		23 33 31	27 39 39	
g_{FS}	Forward Transconductance	V_{DS} = –5 V, I_D = – 4.2 A V_{DS} = 5 V, I_D = 5.9 A	Q1 Q2		13 23		S
Dynamic Characteristics							
C_{iss}	Input Capacitance	Q1: V_{DS} = –10 V, V_{GS} = 0 V, f = 1.0 MHz Q2: V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz	Q1 Q2		753 677		pF
C_{oss}	Output Capacitance		Q1 Q2		163 171		pF
C_{rss}	Reverse Transfer Capacitance		Q1 Q2		83 91		pF
R_G	Gate Resistance	V_{GS} = 15mV, f = 1.0 MHz	Q1		8		Ω
			Q2		2.2		
Switching Characteristics							
$t_{d(on)}$	Turn-On Delay Time	Q1: V_{DD} = –10 V, I_D = –1 A, V_{GS} = –4.5 V, R_{GEN} = 6 Ω Q2: V_{DD} = 10 V, I_D = 1 A, V_{GS} = 4.5V, R_{GEN} = 6 Ω	Q1 Q2		13 11	23 20	ns
t_r	Turn-On Rise Time		Q1 Q2		8 16	16 29	ns
$t_{d(off)}$	Turn-Off Delay Time		Q1 Q2		26 18	42 32	ns
t_f	Turn-Off Fall Time		Q1 Q2		14 7	52 14	ns
Q_g	Total Gate Charge	Q1: V_{DS} = –10 V, I_D = –4.2 A, V_{GS} = –4.5V Q2: V_{DS} = 10 V, I_D = 5.9 A, V_{GS} = 4.5 V	Q1 Q2		7 6	10 8	nC
Q_{gs}	Gate-Source Charge		Q1 Q2		1.6 1.5		nC
Q_{gd}	Gate-Drain Charge		Q1 Q2		1.9 1.8		nC

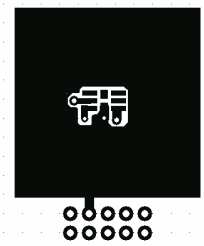
Electrical Characteristics (continued)

T_A = 25°C unless otherwise noted

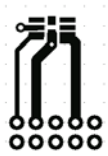
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Drain-Source Diode Characteristics and Maximum Ratings							
I_S	Maximum Continuous Drain-Source Diode Forward Current		Q1 Q2			–1.3 1.3	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = –1.3 A (Note 2) V_{GS} = 0 V, I_S = 1.3 A (Note 2)	Q1 Q2		–0.8 0.7	–1.2 1.2	V
t_{rr}	Diode Reverse Recovery Time	I_F = – 4.2A,d_{IF}/d_t = 100 A/μs I_F = 5.9A, d_{IF}/d_t = 100 A/μs	Q1 Q2		17 15		nS
Q_{rr}	Diode Reverse Recovery Charge	I_F = – 4.2A,d_{IF}/d_t = 100 A/μs I_F = 5.9A, d_{IF}/d_t = 100 A/μs	Q1 Q2		6 4		nC

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 68°C/W when mounted on a 1in^2 pad of 2 oz copper (Single Operation).



b) 102°C/W when mounted on a minimum pad of 2 oz copper (Single Operation).

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%

Typical Characteristics : Q1

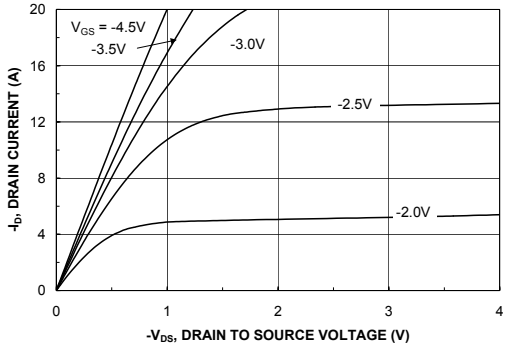


Figure 1. On-Region Characteristics.

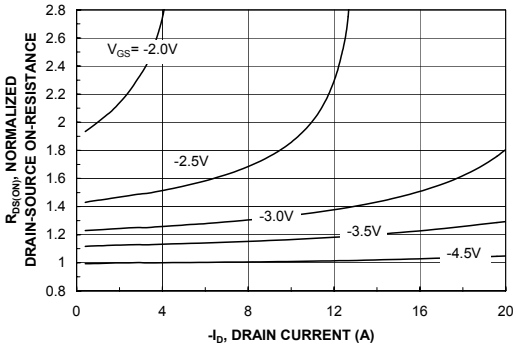


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

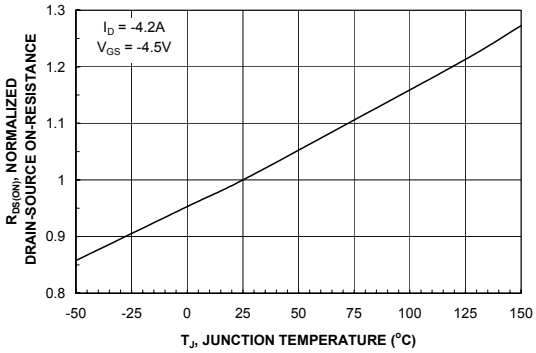


Figure 3. On-Resistance Variation with Temperature.

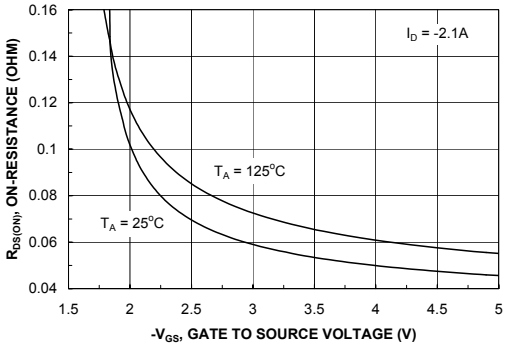


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

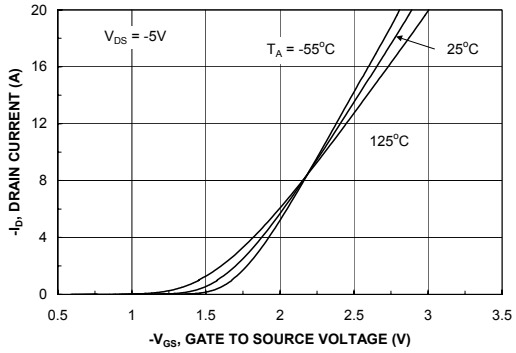


Figure 5. Transfer Characteristics.

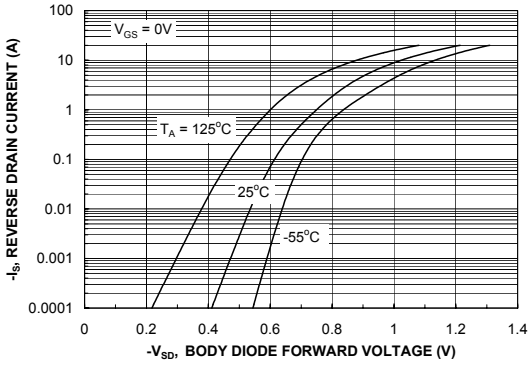


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics : Q1

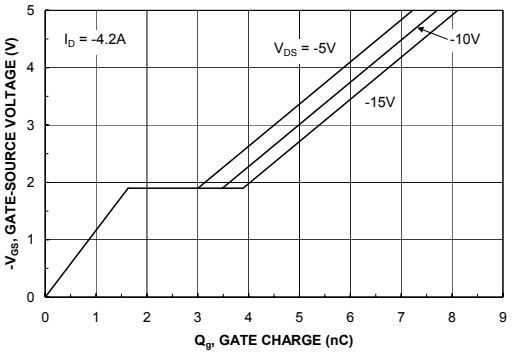


Figure 7. Gate Charge Characteristics.

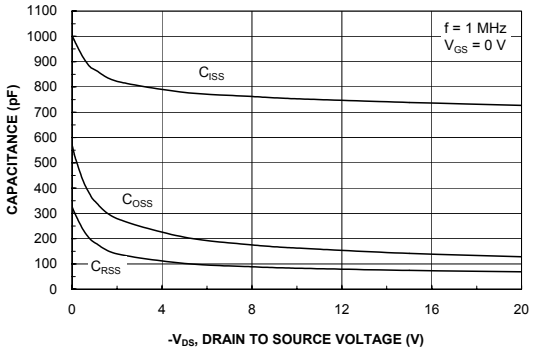


Figure 8. Capacitance Characteristics.

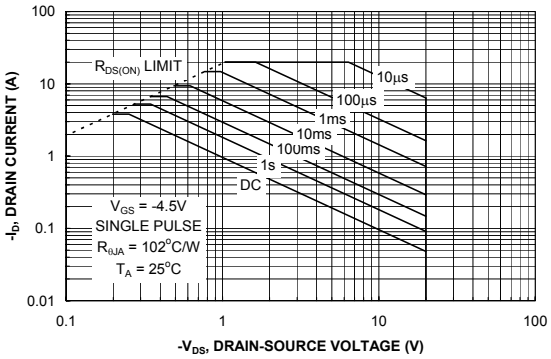


Figure 9. Maximum Safe Operating Area.

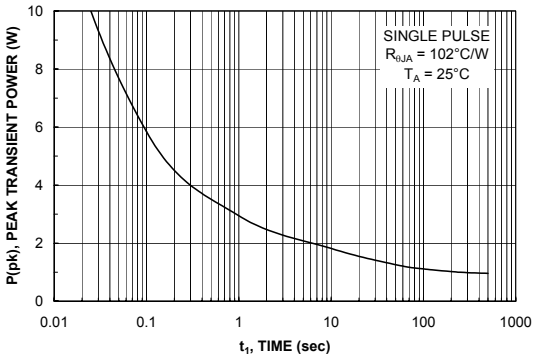


Figure 10. Single Pulse Maximum Power Dissipation.

Typical Characteristics : Q2

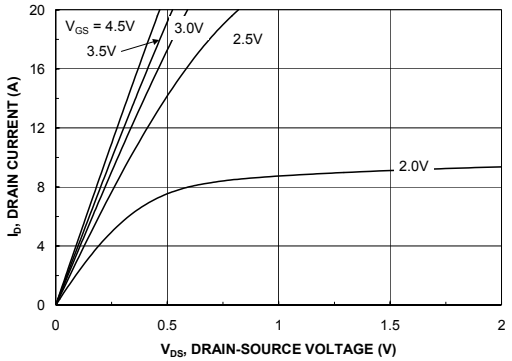


Figure 11. On-Region Characteristics.

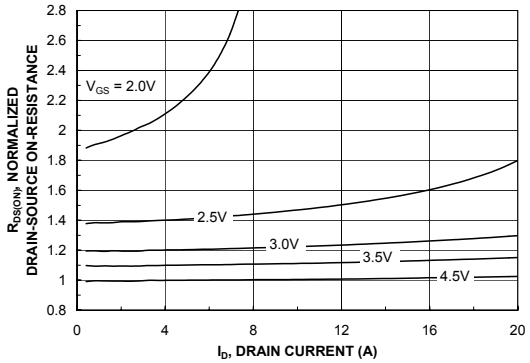


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.

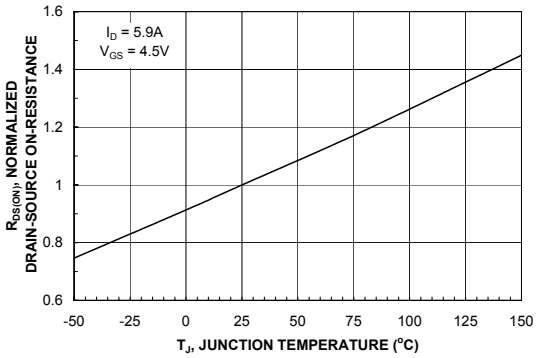


Figure 13. On-Resistance Variation with Temperature.

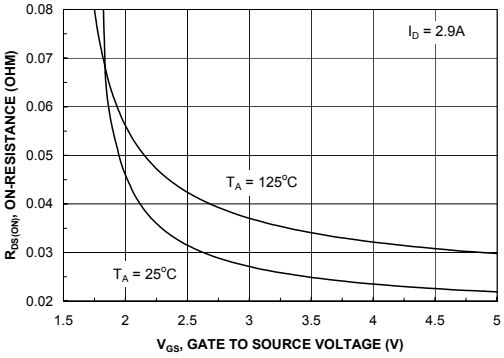


Figure 14. On-Resistance Variation with Gate-to-Source Voltage.

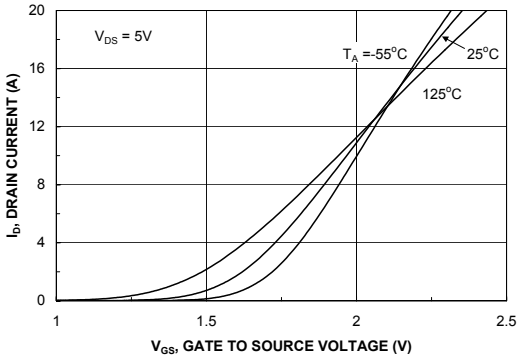


Figure 15. Transfer Characteristics.

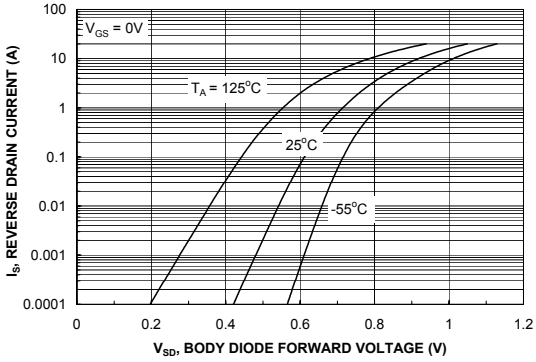


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics : Q2

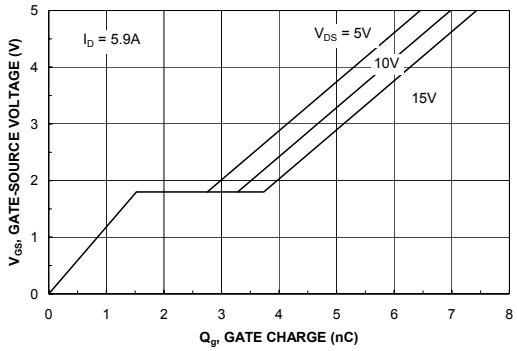


Figure 17. Gate Charge Characteristics.

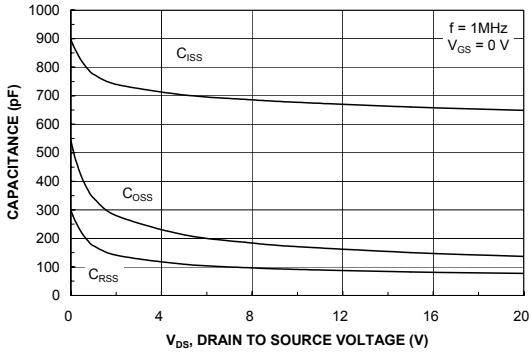


Figure 18. Capacitance Characteristics.

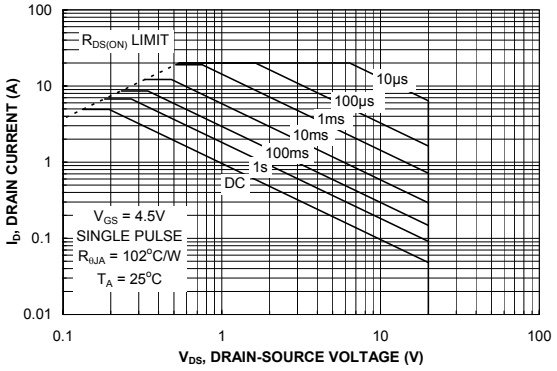


Figure 19. Maximum Safe Operating Area.

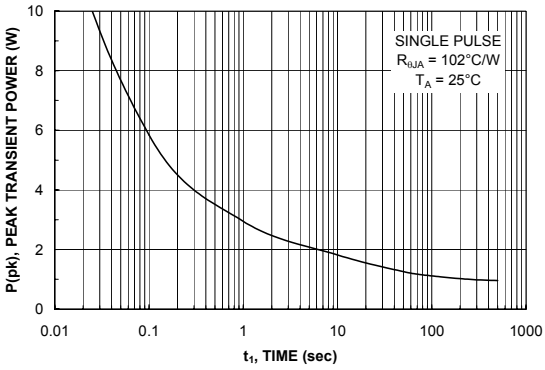


Figure 20. Single Pulse Maximum Power Dissipation.

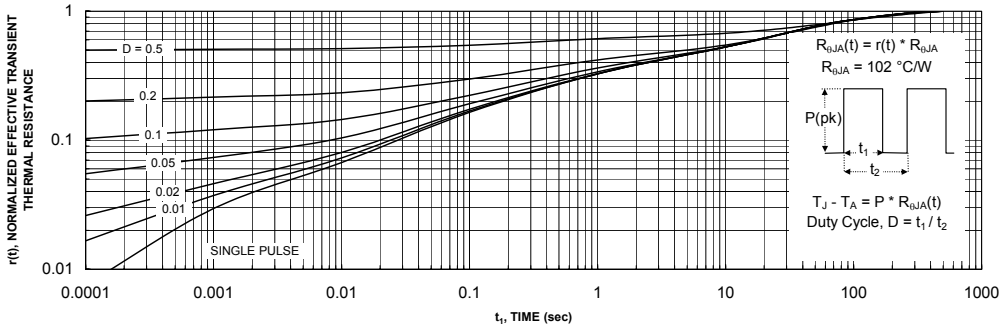
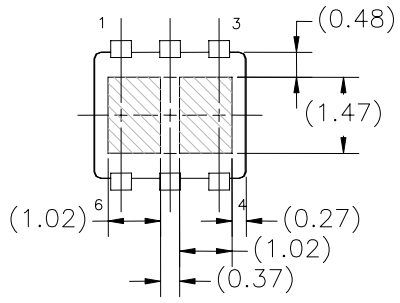


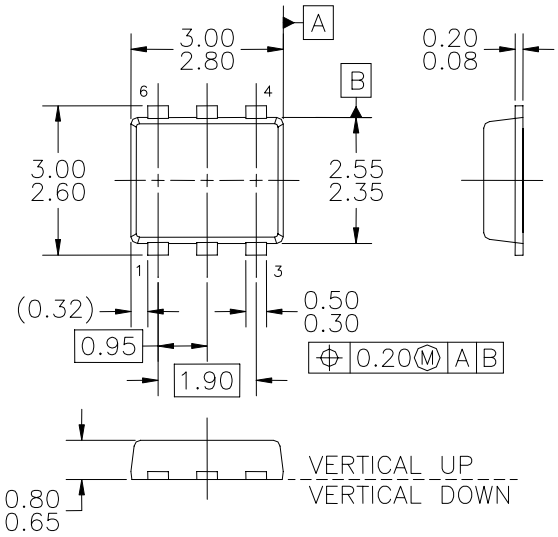
Figure 21. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

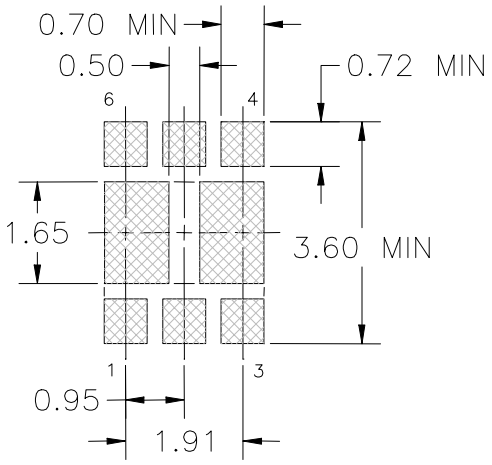
Dimensional Outline and Pad Layout



Bottom View



Top View



Recommended Landing Pattern

For Standard Dual Configuration

NOTES: UNLESS OTHERWISE SPECIFIED

ALL DIMENSIONS ARE IN MILLIMETERS.

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CoolFET™	FRFET™	MicroPak™	QS™	TinyLogic®
CROSSVOLT™	GlobalOptoisolator™	MICROWIRE™	QT Optoelectronics™	TINYOPTO™
DOME™	GTO™	MSX™	Quiet Series™	TruTranslation™
EcoSPARK™	HiSeC™	MSXPro™	RapidConfigure™	UHC™
E^{2}CMOS™	I^{2}C™	OCX™	RapidConnect™	UltraFET®
EnSigna™	ImpliedDisconnect™	OCXPro™	SILENT SWITCHER®	VCX™
FACT™	ISOPLANAR™	OPTOLOGIC®	SMART START™	
Across the board. Around the world.™		OPTOPLANAR™	SPM™	
The Power Franchise™		PACMAN™	Stealth™	
Programmable Active Droop™		POP™	SuperSOT™-3	

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

FDC6020C

Complementary PowerTrench MOSFET Recommend FDC6020C_F077

Contents

BUY

Datasheet

Download this datasheet

e-mail this datasheet

This page

Print version

This product

Use in FETBench Analysis

Related Links

- Request samples
- How to order products
- Product Change Notices (PCNs)
- Support
- Sales support
- Quality and reliability
- Design center

General description

These N & P-Channel MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

back to top

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  - $R_{DS(ON)}$ = 55 mΩ @ V_{GS} = -4.5V
  - $R_{DS(ON)}$ = 82 mΩ @ V_{GS} = -2.5V
- Q2 5.9A, 20V
  - $R_{DS(ON)}$ = 27 mΩ @ V_{GS} = 4.5V
  - $R_{DS(ON)}$ = 39 mΩ @ V_{GS} = 2.5V
- Low gate charge
- High performance trench technology for extremely low $R_{DS(ON)}$
- FLMP SSOT-6 package: Enhanced thermal performance in industry-standard package size

back to top

Applications

- DC/DC converter
- Load switch
- Motor Driving

back to top

Product status/pricing/packaging BUY

Product	Product status	Pb-free Status	Pricing*	Package type	Leads	Packing method	Package Marking Convention**
FDC6020C	Not recommended for new designs		$0.38	SSOT-6 FLMP	6	TAPE REEL	Line 1: &E&**Y** (Binary Calendar Year Coding) Line 2: .020
FDC6020C_F077	Full Production	Full Production	$0.57	SSOT-6 FLMP	6	TAPE REEL	Line 1: &E&**Y** (Binary Calendar Year Coding) Line 2: .020

* Fairchild 1,000 piece Budgetary Pricing
** A sample button will appear if the part is available through Fairchild's on-line samples program. If there is no sample button, please contact a Fairchild distributor to obtain samples

Indicates product with Pb-free second-level interconnect. For more information click here.

Package marking information for product FDC6020C is available. Click here for more information .

back to top

Models

Package & leads	Condition	Temperature range	Software version	Revision date
PSPICE				
SSOT-6 FLMP-6	Electrical	25°C to 125°C	Orcad 9.1	Apr 20, 2004

back to top

Qualification Support

Click on a product for detailed qualification data

Product

FDC6020C

FDC6020C_F077

back to top